High Step-up DC-DC Converter for Fuel Cell Vehicles Based on Merged Quadratic Boost-Ćuk

V. Fernão Pires, *Senior Member, IEEE*, Armando Cordeiro, Daniel Foito and J. Fernando Silva, *Senior Member, IEEE*

***Abstract*— Most fuel cell electric vehicles (*FCEV*) require wide voltage-gain *DC-DC* converters to increase and equalize the relatively low voltage of fuel cell stacks with *DC* link bus or energy storage devices (*ESD*), such as supercapacitors or batteries. This paper proposes two new non-isolated *DC-DC* converters suitable for such applications, which can be extended to other electric vehicles as well. The proposed converters combine the main characteristics of both quadratic Boost and Ćuk converters, offering high step-up voltage and control simplicity using only one ground referenced active power switch. Additionally, the proposed topologies present reduced voltage stress across the active power switch when compared to other Boost converters. Considerations about the design of the proposed converters will also be presented. Experimental results obtained using a laboratory prototype validate the effectiveness and feasibility of the proposed topologies and its suitability for fuel cell electric vehicles.**

***Index Terms*— Fuel cell electric vehicles, single-switch, wide voltage-gain, non-isolated converter, quadratic Boost and Ćuk converters, low voltage stress.**

I. INTRODUCTION

The transportation sector is of vital importance for modern society, economically and socially. Given its importance it is almost impossible to globally reduce the number of transportation vehicles on the roads, oceans and skies despite the environmental problems created by their massive use. To reduce critical levels of pollution, especially in big cities, many countries have adopted restricted policies to the use of internal combustion engines. These restrictive policies, often associated with some tax incentives over the last years, steered major automotive manufacturers to increase the investment in the development and commercialization of hybrid (*HEV*), plug-in hybrid (*PHEV*) and full electric vehicles (*FEV*) [1]-[4]. Lots of research work has been carried over the last decade in the electrification of road vehicles to create efficient, safe, reliable and economically viable solutions. Electric vehicle research has been mainly focused on the design and optimization of energy storage devices (*ESDs*) [5]-[7], power electronics for energy conversion on-board [8]-[15], design of powertrain component types and sizes [16], [17] optimal control strategies [18], [19], battery chargers [20], [21], grid charging management [1], [22], [23], among other aspects.

Fuel-cell (*FC*) vehicles are considered a promising solution that have the potential to provide clean propulsion power. Some electric vehicles powered by hydrogen FCs can be found in the market, however, the use of fuel cells brings certain challenges that must be overcome. Hydrogen is flammable and explosive, and its storage requires special precautions. Additionally, the price of high-power FCs is still high and appropriate hydrogen fueling infrastructures must be created [7] [24] [25]. *FCs* are non-linear low-voltage current intensive power sources that must be stacked to achieve high voltage output. Due to lifetime reasons and reliability the typical output voltage is usually limited to 100 V. Nevertheless, the *DC* bus link of FC vehicles typically need voltages around 250-400V [7], [10], [13].

Power converters play an important role in FC applications providing the required wide voltage-gain to connect the stacks to the *DC* bus link. The conventional *DC-DC* Boost converter is usually unsuitable for this purpose as it presents some limitations, such as, low efficiency at high duty cycle ratio, high frequency losses, reverse recovery problems in power semiconductors with reduced efficiency [9], [26]. Additionally, a recent study revealed that the lifetime of fuel cells is affected by the input current ripple of the Boost converter [27]. To overcome these problems several *DC-DC* Boost topologies have been proposed to increase the voltage level of the *FC* stacks. Some of the most well-known *DC-DC* Boost converter are based on three-level [28], [29], hybrid [30], multilevel [31], [32], switched-inductor [33], [34], switched-capacitor [35], [36], cascaded [37], [38], coupled inductors [39], [40], Z source network [41], Quasi-Z source network [42] and parallel resonant [43]. Other applications for these converters are the distributed generation systems

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(*DGSs*), *ESDs* and renewable energy sources (*RES*).

Some of the *DC-DC* Boost converters proposed do not provide wide voltage-gain, low voltage stress for power switches and reduced input current ripple at the same time. Therefore, two new non-isolated high step-up Boost converters with quadratic gain characteristics are proposed for multiphase *FC* converters to reduce input current ripple and increase power handling capability. Each *FC* converter phase is based on the quadratic Boost and Ćuk converters (*HQBC*). They have been designed to offer a very high voltage gain. Moreover, *HQBCs* are also characterized by a single active power semiconductor and reduced voltage stress across all the power semiconductors. The design and analysis of the proposed *HQBCs* will be addressed. Results from a laboratory prototype will confirm the effectiveness and feasibility of the proposed topologies and its suitability for *FC* electric vehicles.

II. Circuit Configuration

Quadratic Boost *DC-DC* converters have been used and studied due to their high voltage gain characteristics. This converter is characterized by a simple structure using a single active switch (Fig. 1). However, the switch hold-off voltage equals the output voltage. Additionally, in real applications there is some limitation regarding the voltage gain, due to parasitic resistors and on-state voltage drops. Thus, new *DC-DC* converters characterized by extended voltage gains (compared to the quadratic Boost) are here proposed. The power topology of the first proposed converter is presented in Fig. 2 and termed *HQBC* (from Hybrid *QBC*) type I. The *HQBC* topology can be obtained by merging a quadratic Boost with a Ćuk converter, while still maintaining the need to use just a single active switch per phase. Through the analysis of the *HQBC* type I topology is also possible to see that the voltage stress that the active switch must withstand is lower than the output voltage of the converter. Another proposed topology derived from the quadratic Boost is presented in Fig. 3 and termed *HQBC* type II. This topology presents similar characteristics as the *HQBC* type I (Fig. 2). It also requires only a single active switch with a reduced blocking voltage stress. As will be seen, *HQBC* type II is characterized by higher voltage gain when compared with the *HQBC* type I presented in Fig. 2.

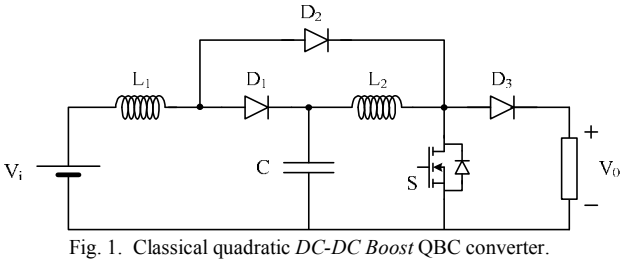


Fig. 1. Classical quadratic *DC-DC Boost* QBC converter.

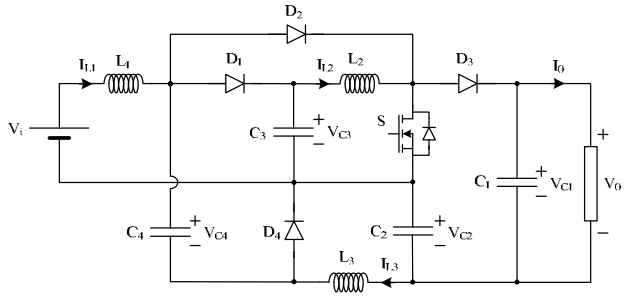


Fig. 2. Proposed quadratic DC-DC *Boost-Ćuk* HQBC converter type I.

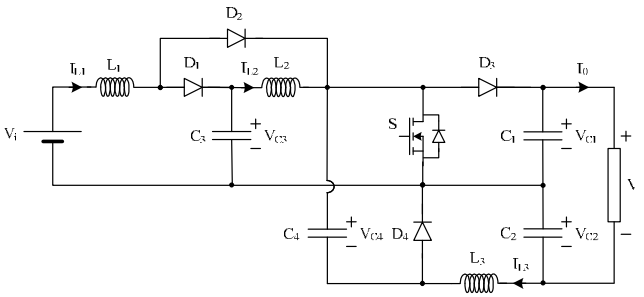


Fig. 3. Proposed quadratic *DC-DC Boost-Ćuk HQBC* converter type II.

The study of both *HQBC* converters reveals that in steady state they can present two modes of operation: continuous conduction mode (*CCM*) and discontinuous conduction mode (*DCM*). For fuel cell operation the *CCM* mode can enable nearly constant input current in multiphase topology and is therefore analyzed in the following subsections.

III. Principle of Operation and Analysis in *CCM*

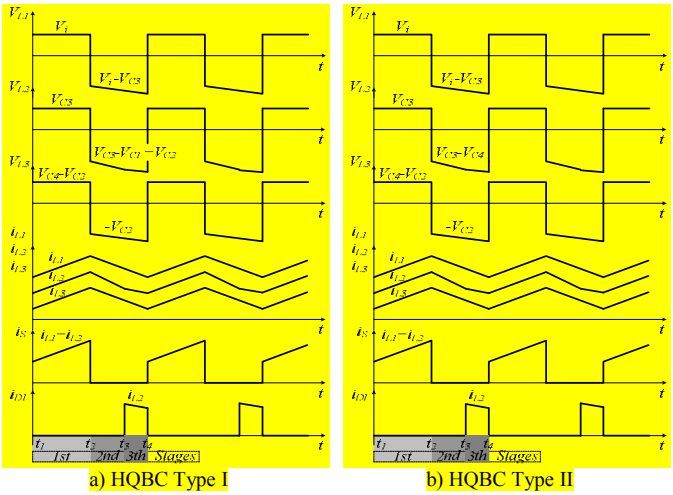
The principle of operation of the two proposed converters is similar as shown in Fig. 4. Therefore, the converter *HQBC* type I will be used to analyze both *HQBC* topologies. The switching period of the converter *HQBC* type I operating in *CCM* is divided in three-time intervals, as shown in Fig. 4 b), described hereafter:

1) Interval [t_1-t_2] (corresponding to fig. 5 a): In the instant t_1 the switch *S* turns on starting the 1st stage and finishing the previous transient process. The energy from the *DC* source and capacitors C_3 and C_4 starts to be transferred to inductors L_1, L_2 and L_3, increasing their respective currents. Diodes D_1, D_3 and D_4 will be turned off since they are reverse biased (V_{C2}-V_{C1}, -V_{C3} and -V_{C4} respectively).

2) Interval [t_2-t_3] (corresponding to fig. 5 b): This sub-interval is associated to the 2nd stage and started with the turn-off of switch *S*. The energy stored in the inductors L_1, L_2 and L_3 will be transferred to capacitors C_1 and C_4, decreasing the inductor currents. It should be noted that this process happens only when the voltages across the capacitors C_4 and C_3 obey $V_{C4} < V_{C3}$, as diode D_3 is still reverse biased since the applied voltage remains negative (V_{C4}-V_{C3}).

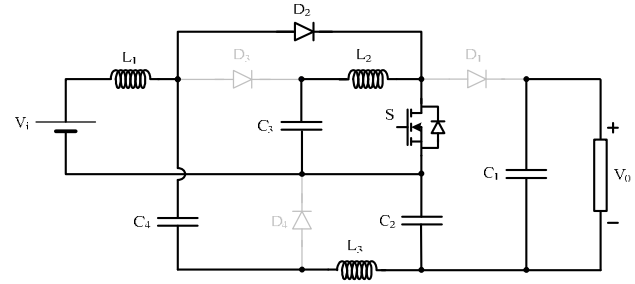
3) Interval [t_3-t_4] (corresponding to fig. 5 c): In this sub-interval (3th stage) switch *S* is still turned off, but now $V_{C4} > V_{C3}$. Being the voltage at the terminals of capacitor C_3 smaller than the voltage at the terminals of capacitor C_4, D_3 is

not anymore reverse biased and conducts. The energy stored in inductor L_1 will be transferred to capacitor C_3, while inductors L_2 and L_3 will continue to transfer energy to capacitor C_1.

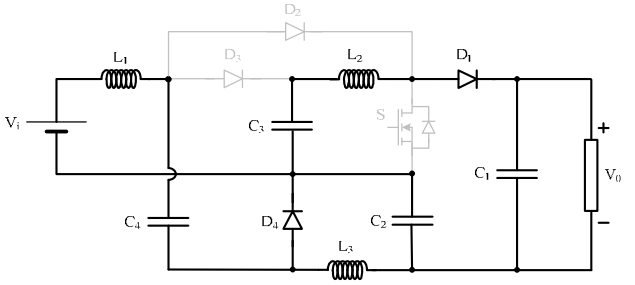


a) HQBC Type I b) HQBC Type II

Fig. 4. Waveforms associated to the power converters operating stages.



a)



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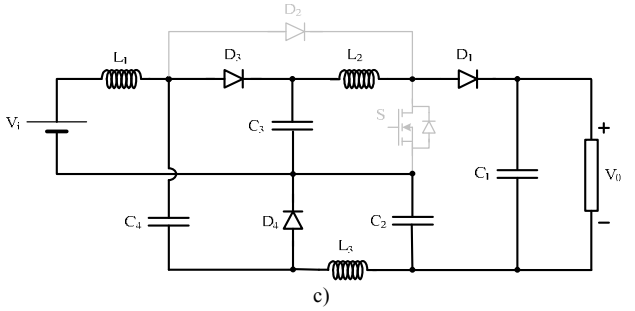

c)

Fig. 5. Equivalent circuits of *HQBC* type II operating in *CCM*.

The *HQBC* type II converter presents the same three sub-intervals when operating in *CCM*. The sub-intervals are similar to the ones explained for the *HQBC* type I converter.

As described before, the existing classic quadratic Boost presents a high steady-state output to input voltage transfer ratio. In fact, the output/input ideal voltage gain V_o/V_i has a quadratic dependence on the switch S duty cycle δ, as shown in (1). Compared to the Boost converter, the classic quadratic Boost gain increases from 3.3 to 11.1 at $\delta = 0.7$.

$$\frac{V_o}{V_i} = \frac{1}{(1-\delta)^2} \tag{1}$$

Regarding the steady-state voltage gain of the *HQBC* type I (Fig. 2) converter operating in *CCM*, it will be considered that all components are ideal. According to this assumption, the waveforms of Fig. 4 a) and considering one switching cycle, the relationship between the output and input current function of the duty cycle, can be obtained through the volt-second relationship in inductors L_1, L_2 and L_3, being respectively:

$$\delta V_i + (1-\delta)(V_i - V_{C_3}) = 0 \tag{2}$$

$$\delta V_{C_3} + (1-\delta)(V_{C_3} - V_{C_1} + V_{C_2}) = 0 \tag{3}$$

$$\delta(V_{C_2} - V_{C_3}) + (1-\delta)V_{C_2} = 0 \tag{4}$$

Noting now that the output voltage is the voltage across capacitor C_1 ($V_o = V_{C1}$) and using the previous relationships the *HQBC* type I output to input voltage transfer ratio is:

$$\frac{V_o}{V_i} = \frac{1+\delta(1-\delta)}{(1-\delta)^2} \tag{5}$$

Comparing (5) and (1) shows that the *HQBC* type I converter increases the voltage gain. The *HQBC* type I gain increases to 13.4 at $\delta = 0.7$, regarding the classic quadratic Boost value of 11.1.

Applying the previous analysis to the *HQBC* type II converter (Fig. 3), the relationship between the output and input voltage is expressed by:

$$\frac{V_o}{V_i} = \frac{1+\delta}{(1-\delta)^2} \tag{6}$$

From the analysis of equation (6) is possible to verify that this last converter presents the highest voltage gain when compared with the classical quadratic Boost and *HQBC* type I. The voltage gain function of the duty cycle of the three power converters can be seen in Fig. 6. In fact, this figure shows that with the proposed power converters the voltage gains for all duty cycles are higher than the classical one.

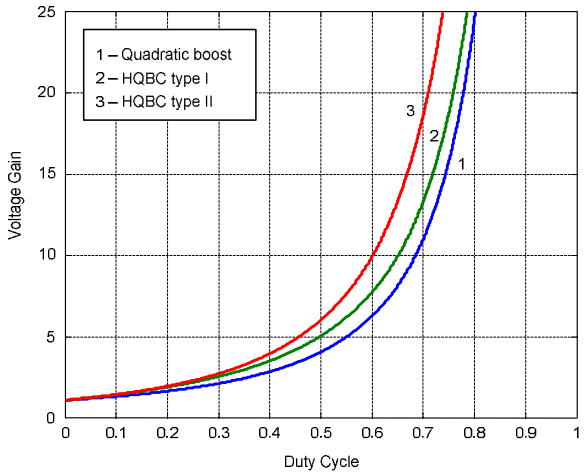

Fig. 6. Static voltage gain versus duty cycle.

Regarding the dynamics of the proposed DC-DC converters, they will present behaviours similar to the classical quadratic converter. Therefore, and taking into consideration a fuel-cell, the proposed converters could be used with open loop or with closed loop controllers. For example, in open loop, the duty-cycle can be determined externally by the fuel cell maximum power point tracking (MPPT) controller. This MPPT controller would smoothly and interactively change the duty-cycle until the desired maximum power point is reached [44]. In closed loop control, supposing it is required to maintain the output voltage at a desired value, a proportional integral (PI) compensator could be used. This PI compensator could be determined, using a similar approach for the classical quadratic Boost as presented, for example in [45]. Other possible closed loop controllers could be a sliding mode controller for the input i_{L1} current and a PI compensator for the output voltage to define the needed i_{L1} current [46].

IV. Voltage and Current Stresses

The voltage and current stresses affecting the semiconductors are function of the output power and voltage defined for the power converter. A straightforward circuit analysis of the *HQBC* type I converter shows that the switch *S* maximum hold off voltage is equal to the peak voltage across the capacitor C_1 minus the minimum voltage across capacitor C_2. Therefore, the voltage stress across the switch *S* is given by equation (7), where V_{C1}, V_{C2} are the average values and ΔV_{C1}, ΔV_{C2} the voltage ripples of C_1, C_2, respectively. The maximum switch current is a function of the operating point of the converter (duty cycle δ) and load current. The maximum switch current is given by equation (8).

$$V_{S\max} = V_{C1} + \frac{\Delta V_{C1}}{2} - V_{C2} - \frac{\Delta V_{C2}}{2} \tag{7}$$

$$I_{Sav\max} = \frac{\left(2\delta + \delta^2 - \delta^3\right) I_o}{(1-\delta)^2} \tag{8}$$

From the above analysis it is possible to realize that the switch presents a voltage stress lower than the power converter output voltage (V_o). However, it requires a higher current stress when compared with the classic quadratic Boost since it must supply current to capacitors C_1 and C_4.

Using the same method, the maximum voltage and current stress of the *HQBC* type II converter switch can be given by (9) and (10). Similar conclusions can be obtained from those equations.

$$V_{S\max} = V_{C1} + \frac{\Delta V_{C1}}{2} \tag{9}$$

$$I_{Sav\max} = \frac{\left(2\delta + \delta^2 + \delta^3\right) I_o}{(1-\delta)^2} \tag{10}$$

Regarding the voltage stress at the terminals of the four diodes of the *HQBC* type I, they can be written in expressions (11). From those expressions it can be concluded that the voltage stresses at the terminals of the four diodes are lower than the output voltage (V_o). Considering the *HQBC* type II the voltage stress at the terminals of the diodes are given by (12).

$$\begin{cases} V_{D2} = V_{C1} + \dfrac{\Delta V_{C1}}{2} - V_{C2} - \dfrac{\Delta V_{C2}}{2} - V_{C3} + \dfrac{\Delta V_{C3}}{2} \\ V_{D3} = V_{C1} + \dfrac{\Delta V_{C1}}{2} - V_{C2} - \dfrac{\Delta V_{C2}}{2} \\ V_{D1,4} = V_{C3} + \dfrac{\Delta V_{C3}}{2} \end{cases} \tag{11}$$

$$\begin{cases} V_{D1} = V_{C3} + \dfrac{\Delta V_{C3}}{2} \\ V_{D2} = V_{C1} + \dfrac{\Delta V_{C1}}{2} - V_{C3} + \dfrac{\Delta V_{C3}}{2} \\ V_{D3} = V_{C1} + \dfrac{\Delta V_{C1}}{2} \\ V_{D4} = V_{C4} + \dfrac{\Delta V_{C4}}{2} \end{cases} \tag{12}$$

The maximum value of the average currents of diodes D_1 to D_4 are given in expressions (13) and (14) for the *HQBC* type I and *HQBC* type II respectively.

$$\begin{cases} I_{D3av\max} = I_{D4av\max} = I_o \\ I_{D2av\max} = \dfrac{\delta(1+\delta) I_o}{(1-\delta)^2} \\ I_{D1av\max} = \dfrac{I_o}{(1-\delta)^2} \end{cases} \tag{13}$$

$$\begin{cases} I_{D3av\max} = I_{D4av\max} = I_o \\ I_{D2av\max} = \dfrac{\delta(1+\delta)I_o}{(1-\delta)^2} \\ I_{D1av\max} = \dfrac{(1+\delta)I_o}{1-\delta} \end{cases} \quad (14)$$

The voltage stress of switch *S* as function of the duty cycle is expressed as a percentage of the output voltage (Fig. 7) for the classical quadratic converter, *HQBC* type I and *HQBC* type II (considering negligible ripple in the capacitor voltages). Fig. 7 also shows that the classic quadratic converter switch must also hold-off the complete output voltage. However, the *HQBC* converter switches must hold-off a lower voltage for duty cycles higher than zero. It can also be pointed out that the *HQBC* type II presents the lowest voltage stresses.

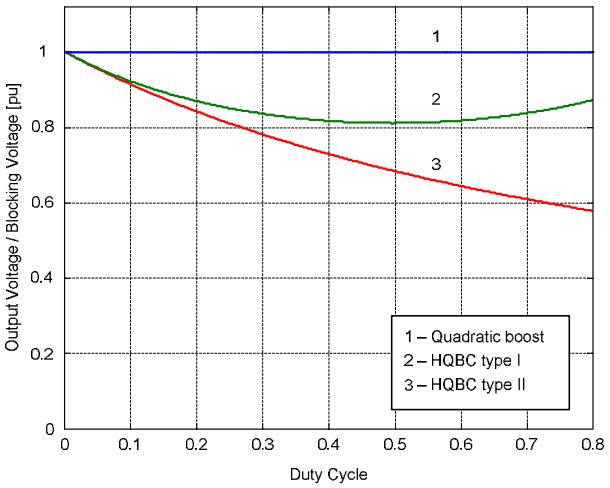

Fig. 7. Blocking voltage that the switch must hold-off function of the duty cycle vs output voltage.

V. SIZING OF PASSIVE COMPONENTS

The passive elements (inductors and capacitors) will be sized considering a given limit for their state variable ripple. For inductors the maximum current ripple Δi_L will be considered as a percentage of the inductor average current. Considering currents with quasi-linear variation, the inductor L_1 of the *HQBC* type I and Δi_{L1} type II topologies can be estimated from the expression of the inductor voltage (V_{L1}) during the switch on time ($\Delta t_{on}=\delta T=\delta/f_{PWM}$), and the ripple ($\Delta i_{L1}$) in the inductor current:

$$\Delta i_{L_1 typI} = \delta \frac{V_i}{L_1 f_{PWM}} = \delta \frac{(1-\delta)^2}{1+\delta(1-\delta)} \frac{V_o}{L_1 f_{PWM}} \quad (15)$$

$$\Delta i_{L_1 typII} = \delta \frac{V_i}{L_1 f_{PWM}} = \delta \frac{(1-\delta)^2}{1-\delta} \frac{V_o}{L_1 f_{PWM}} \quad (16)$$

Analyzing (15) and (16) the maximum value for inductor L_1 is found for $\delta = 0.31$ and $\delta = 0.28$ for the *HQBC* types I and II respectively:

$$L_{1\max typI} = 0.31 \frac{V_o}{\Delta i_{L_1} f_{PWM}} \quad (17)$$

$$L_{1\max typII} = 0.28 \frac{V_o}{\Delta i_{L_1} f_{PWM}} \quad (18)$$

Therefore, the *HQBC* type II converter requires a lower inductance value.

For the inductors L_2, using a similar analysis it may be found that the maximum values are for $\delta = 0.5$ and $\delta = 0.41$ respectively for *HQBC* types I and II. Thus, these inductors can be determined by equations (19) and (20). Again, the *HQBC* type II converter requires a lower inductance value

$$L_{2\max typI} = 0.5 \frac{V_o}{\Delta i_{L_2} f_{PWM}} \quad (19)$$

$$L_{2\max typII} = 0.41 \frac{V_o}{\Delta i_{L_2} f_{PWM}} \quad (20)$$

Inductor L_3 can be determined by a similar analysis using the expression of the inductor voltage (V_{L3}) during the switch on time ($\Delta t_{on}=(1-\delta)/f_{PWM}$). The maximum values of inductors L_3 for *HQBC* type I and type II converters are also obtained for $\delta = 0.5$ and $\delta = 0.41$ respectively. Thus, as in the previous cases the *HQBC* type II require a lower inductance value as can be seen comparing (21) and (22).

$$L_{3\max typI} = 0.5 \frac{V_o}{\Delta i_{L_3} f_{PWM}} \quad (21)$$

$$L_{3\max typII} = 0.41 \frac{V_o}{\Delta i_{L_3} f_{PWM}} \quad (22)$$

Regarding the sizing of capacitors, a similar procedure will be used, considering now a limit for the voltage ripple. Thus, to size capacitor C_1 of the *HQBC* topologies a maximum ripple (ΔV_{C1}) as a percentage of the capacitor average voltage (V_{C1}) is allowed. Supposing a nearly linear voltage variation, from the capacitor voltage value during the switch on time ($\Delta t_{on}=\delta T=\delta/f_{PWM}$), the value of the capacitor C_1 function of the voltage ripple for the *HQBC* type I and II can be expressed by:

$$C_1 = \frac{\delta I_o}{\Delta V_{C_1} f_{PWM}} \quad (23)$$

For the capacitor C_2 of *HQBC* type I, the analysis is similar, returning an equation related to (23), where ΔV_{C1} is replaced by ΔV_{C2}. However, the same capacitor C_2 for the *HQBC* type II, must have a different analysis since the current through this capacitor does not present nearly constant instantaneous values during each conduction state. Thus, this capacitor may be sized considering its charge variation (ΔQ_2)

function of the current variation in inductor L_2 (Δi_{L2}). Consequently, the capacitance value is:

$$C_{2typII} = \frac{\Delta i_{L_2}}{8\Delta V_{C_2} f_{PWM}} \tag{24}$$

To size capacitors C_3, an analysis alike the used for C_1 is made. The values of the capacitor C_3 function of their voltage ripple for the *HQBC* type I and II re respectively:

$$C_{3typI} = \frac{\delta I_o}{(1-\delta)^2 \Delta V_{C_3} f_{PWM}} \tag{25}$$

$$C_{3typII} = \frac{\delta(1+\delta) I_o}{(1-\delta)\Delta V_{C_3} f_{PWM}} \tag{26}$$

Regarding the calculation of the capacitor C_4, using the same procedure the capacitance value for the *HQBC* type I and II is found to be:

$$C_4 = \frac{\delta I_o}{\Delta V_{C_4} f_{PWM}} \tag{27}$$

VI. Experimental Results

To validate the assumptions previously made, two low-power experimental converter setups (*HQBC* type I and *HQBC* type II) were designed and implemented. Both prototypes have nominal power of 250 W, 24 V input voltage, inductors L_1 = 10 mH, L_2 = 10 mH and L_3 = 10 mH, and capacitors $C_1 = C_2$ = 100 µF, C_3 = 40 µF and C_4 = 20 µF. A switching frequency of 20 kHz was used to avoid human audible noise. Selected power semiconductors were the UJC06505K for the MOSFETs, the SCS240AE2HR for the diodes D_1 and D_2 and the VS-60EPU04PbF for the diodes D_3 and D_4. A TDS3014C oscilloscope was used to the acquisition of the waveforms. A photograph of the prototype and the laboratory workbench is presented in Fig. 8. Tests were conducted at duty cycles needed to obtain an output operation at 200 V in both setups.

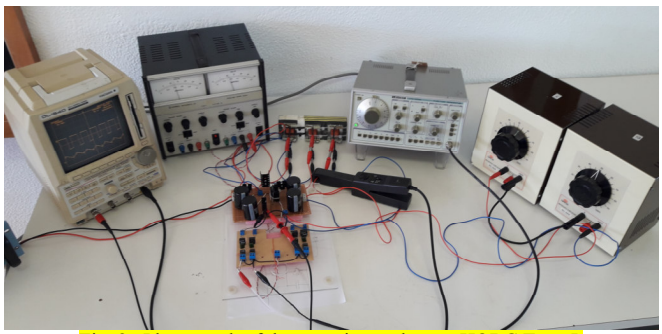

Fig. 8. Photograph of the experimental setup HQBC Type I.

Experimental results obtained with the developed *HQBC* type I laboratory setup using the above parameters are presented in figs. 9-11. The steady-state behavior of the input voltage (V_i), capacitor voltages (V_{C1} and V_{C2}) and the total output voltage of the converter (V_o) is shown in Fig. 9. This figure shows the output voltage nearly equal to 200 V at 24 V input voltage. This output voltage was obtained with a duty cycle of 0.64 confirming the expected gain of this converter. There is a small difference between the theoretical and experimental results that is related with ON-state voltage drops around 3 V in the active switch, diodes and inductor parasitic resistors which were not considered in the theoretical analysis. Through the voltage value in the capacitors C_2 and C_3 it is also possible to confirm that the V_{C2} voltage is about 1.5 times higher than the V_{C3} voltage.

Fig. 10 displays the time behavior of the voltages across switch S and across diodes D_1, D_2 and D_4. These results can be used to note that the voltage across the switch is 20% smaller than the output voltage. Voltages across all the diodes are also lower than the output voltage, presenting a reduction of 70 % for the diode D_2. The currents in the inductors i_{L1}, i_{L2} and i_{L3} can be seen in Fig. 11. This confirms the theoretical analysis where the input current (i_{L1}) is higher than the currents in the inductors L_2 and L_3. Regarding the spikes that can be seen during the transition, are due to the non-ideality of the circuit implementation. Despite the details considered in the design of the circuit there are always parasitic elements, such as inductances or capacitances that are extremely difficult to eliminate entirely. Even the minimum distance between the physical connection of the transistor, diodes and capacitors results in inductor current spikes.

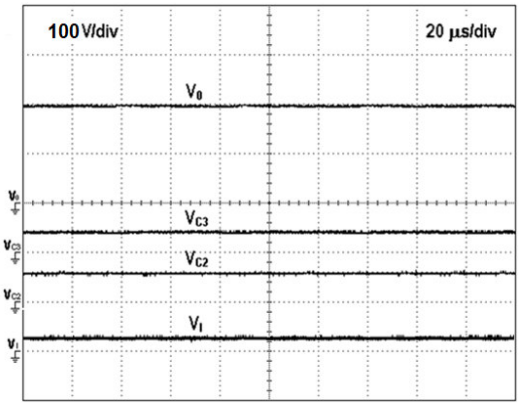

Fig. 9. Experimental results of the quadratic *DC-DC Boost-Ćuk* converter *HQBC* type I – voltage waveforms of V_i, V_{C2}, V_{C3} and V_o.

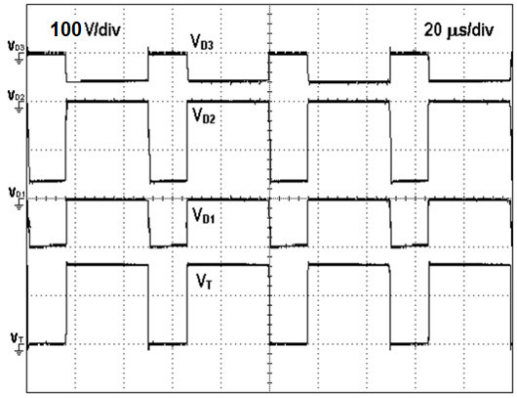

Fig. 10. Experimental results of the quadratic *DC-DC Boost-Ćuk* converter *HQBC* type I – voltage waveforms across switch *S* and diodes D_1, D_2 and D_4.

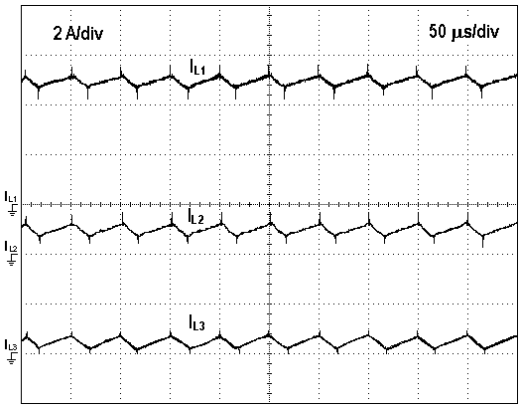

Fig. 11. Experimental results of the *DC-DC HQBC* type I converter – current waveforms in the inductors i_{L1}, i_{L2} and i_{L3}.

Tests were also performed for the *HQBC* type II converter setup. Fig. 12 presents the steady-state behavior of the input voltage (V_i), capacitor voltages (V_{C1} and V_{C2}) and the converter output voltage (V_o). This figure shows that the relationship between the input and output voltage is similar as in the *HQBC* type I. However, the output voltage was obtained with a reduced duty cycle ($\delta = 0.6$), confirming the higher gain of the *HQBC* type II topology. The voltage values in capacitors C_1 and C_2 show that the V_{C1} voltage is about 1.7 times higher than the V_{C2} voltage. The experimental time behavior of the voltages across switch *S* and diodes D_1, D_2 and D_4 are presented in Fig. 13. The voltage across the switch (V_T) is 36% lower compared to the output voltage. This result confirms that the voltage across the switch in the *HQBC* type II converter is lower compared to the *HQBC* type I converter. The voltages across the diodes are also lower than the output voltage, presenting a reduction of 65 % for the diode D_3. In Fig. 14 the currents in inductors i_{L1}, i_{L2} and i_{L3} are presented qualitatively confirming the theoretical analysis since the input current (i_{L1}) is higher than currents in the inductors L_2 and L_3.

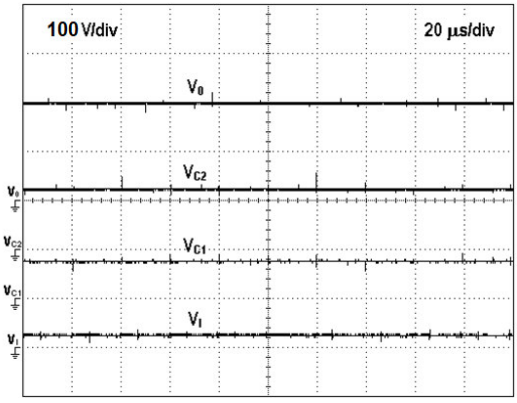

Fig. 12. Experimental results of the *HQBC* type II – voltage waveforms of V_i, V_{C2}, V_{C3} and V_o.

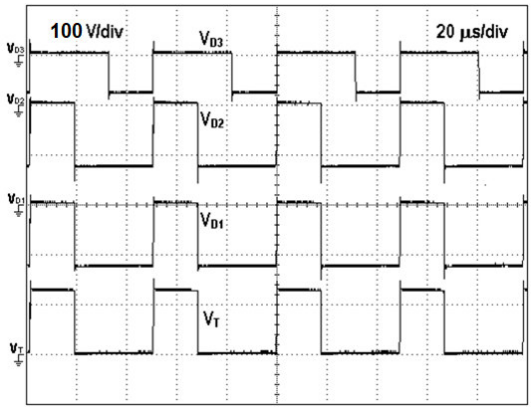

Fig. 13. Experimental results of the of the *HQBC* type II– voltage waveforms across switch *S* and (V_T) diodes D_1, D_2 and D_4.

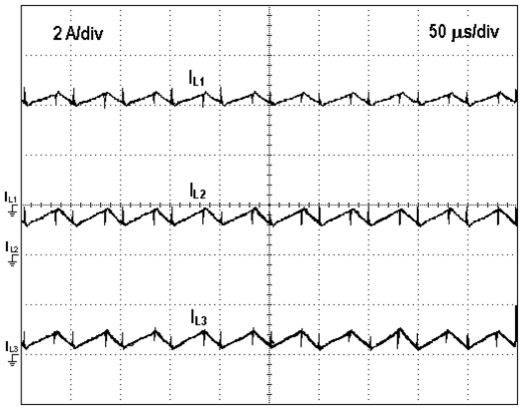

Fig. 14. Experimental results of the of the *HQBC* type II – current waveforms in the inductors i_{L1}, i_{L2} and i_{L3}.

Considering the conditions of the previous tests and achieved results, several experiments were also performed in order to obtain the efficiency of the proposed converters. For the operation of the converters at different output powers, the efficiency curves are presented in Fig. 15. In general, the proposed *HQBC* type I allows slightly higher efficiencies when compared with the proposed *HQBC* type II, the difference increasing slightly for higher powers. It is also possible to verify that maximum efficiencies of 94 % and

93.7 % were obtained for the *HQBC* type I and *HQBC* type II, respectively, considering a constant 24 V input voltage. The efficiency of the classical quadratic Boost converter is also included in this figure (Fig. 15). From this result it can be concluded that the proposed converters have efficiencies similar or slightly lower than the classic quadratic Boost. However, it should be stated that the tests were not made at exactly the same conditions, as it was not possible to obtain the same voltage gain in the quadratic Boost due to the non-ideal components. The quadratic Boost efficiency was measured at 180 V instead of the 200 V output voltage.

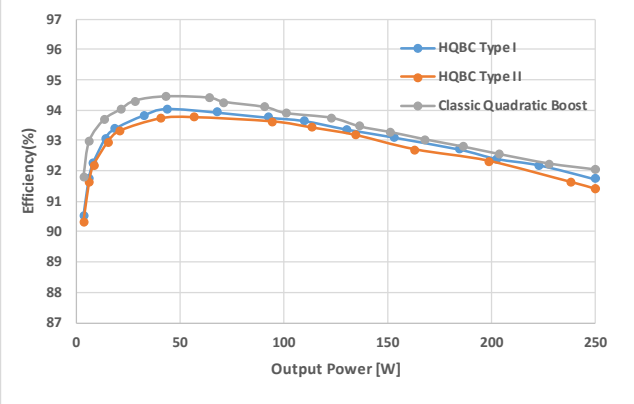

Fig. 15. Efficiency of *HQBC* type I, type II and classical quadratic Boost versus output power.

Besides the presentation of the overall power losses that can be obtained from the converters efficiency, a study about the power-loss breakdown was also made. This important study points out the components that dominate the power-loss amongst the components of the power converters. For the determination of the several losses, a similar approach to the presented in work [47] was used. Fig. 16 presents the power-loss breakdown at the nominal power output, considering power semiconductors conduction and switching losses, magnetic devices losses and other losses (wire losses, temperature dependent losses in power components, skin and proximity effect losses, capacitors equivalent series resistances). The gate-drive and control circuit losses were not considered. The results presented in Fig. 16 show that the majority of the losses are associated with the power semiconductor devices, being 38 % and 39 % for the Type I and Type II, respectively. The conduction losses are higher than the switching losses. Through this study it also possible to verify that the power losses distribution is similar in both proposed topologies.

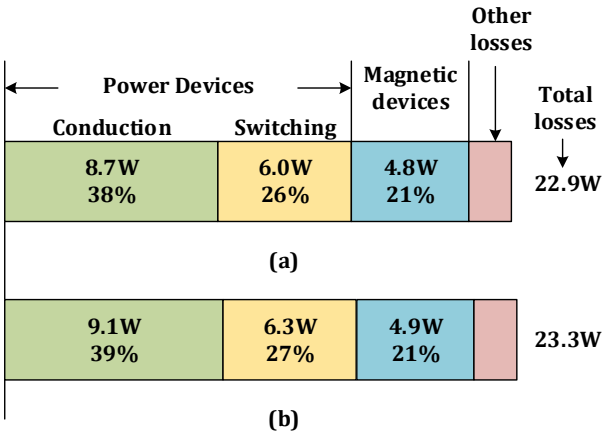

Fig. 16. Power-Loss Breakdown at 200V 250W 20 kHz operation: *HQBC* Type I (a) and *HQBC* Type II (b)

The voltage gain function of the duty cycle of the proposed power converters was also verified through experimental tests. Fig. 17 shows the obtained experimental results. From these results is possible to verify that considering a duty cycle of 0.5 it was obtained voltage gains of 4.8 and 5.6 for the *HQBC* type I and II, respectively. Comparing with the ones obtained through theoretical results (eq. 5 and eq. 6) it is possible to verify that they are slightly lower. However, as mentioned before this difference is due mainly to the semiconductor ON-state voltage drops.

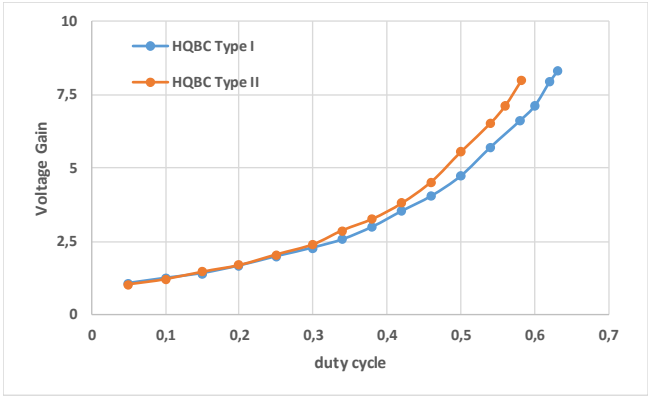

Fig. 17. Experimental voltage gain of *HQBC* type I and type II versus duty cycle.

To further verify the efficiency of the power converter under light load and heavy load operation, a Horizon 200 W PEM Fuel Cell (PEMFC) was used. The polarization curve of this PEM fuel cell can be seen in Fig. 16. For light loads (1 A and 27.1 V) efficiencies of 94.07 % and 94.02 % were obtained for the *HQBC* type I and II, respectively. Regarding heavy loads (11 A and 18.0 V) the efficiencies were lower, namely 89.5 % and 89.2 % for *HQBC* type I and II, respectively. The reduction of this efficiency is essentially due to the reduction of the input voltage that reduces from 27.1 V to 18.0 V.

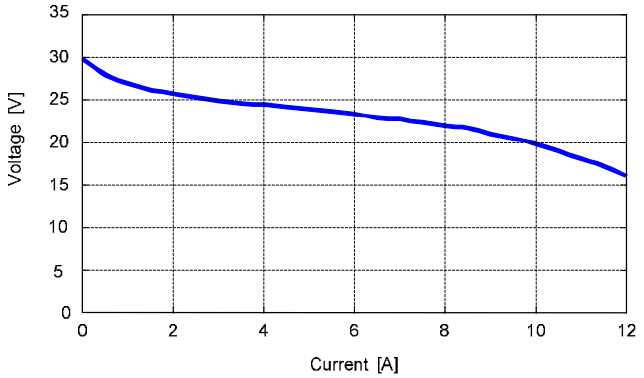

Fig. 18. PEMFC polarization curve.

VII. CONCLUSIONS

This paper addressed the development and the design of new non-isolated *DC-DC* topologies with high step-up voltage gain for multiphase fuel cell applications. The two new *HQBC* topologies were derived merging existing converters that can boost the input voltage. The *HQBC* type I and type II topologies were obtained by integrating both a quadratic Boost and a Ćuk converter around a single active power switch. Therefore, they both maintain the drive simplicity offered by a ground referenced single switch. Additionally, the new *DC-DC HQBC* converters are characterized by increased voltage gains (compared to the quadratic Boost). A straightforward theoretical development was made to characterize the gain and voltage stress of semiconductors of *HQBC* topologies. This study showed a reduction on the voltage stress across the power switch when compared to the output voltage, or the quadratic Boost. The reduction reaches 36 % for the *HQBC* type II active switch and 65 % in some diodes. Equations to size the *HQBC* converters reactive components were also derived. The theoretical results and switching performance were verified using *HQBC* converter type I and type II laboratorial prototypes. The experimental results allowed to verify the operation of the proposed circuits. They also confirmed the high gains of the *HQBC* converters and that they are very similar than the ones obtained by the theoretically predicted. The difference of these values is due to the conduction voltage drops in the active switch, diodes and inductor parasitic resistors.

ACKNOWLEDGMENT

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