- **Real-time motion estimation based on the Full-Search Block-Matching (FSBM) algorithm**
- **New and highly efficient type I single array architecture combined with the traditional pipelining and parallel processing techniques**
- **Fully parameterizable architecture according to a restricted set of setup parameters**
- **Typical application: motion estimator block of typical video CoDecs for ITU-T H.26x and ISO MPEG video coding standards**

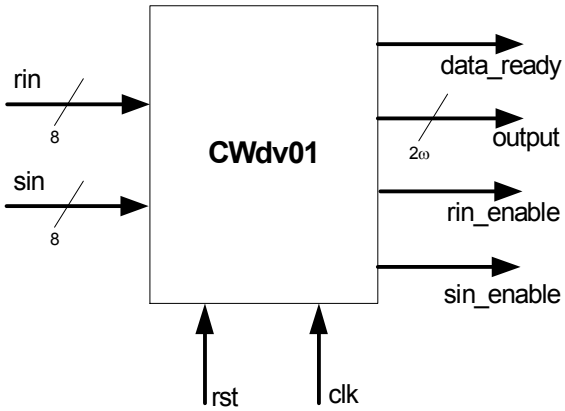

Figure 1. CWdv01 symbol and interface signals.

Description

The CWdv01 is a configurable motion estimation processor based on the full-search block-matching (FSBM) algorithm, designed for real-time operation.

The processor combines a new and highly efficient type I single array processing structure, providing for minimum latency, maximum throughput and full utilization of hardware resources. These features are achieved by applying the traditional pipelining and parallel processing techniques to speed up the data processing. Moreover, it is based on a fully parameterizable multiple array architecture, which allows the implementation of custom processors according to a restricted set of setup parameters to adjust the required performance levels to the available hardware resources.

The processing of the data is initiated as soon as the *rst* signal is released low. In the subsequent N×N clock cycles (where N is the macroblock width) the *rin_enable* and *sin_enable* signals are both active ('1'), so that the pixels of the reference area and of the first slice of the search area are transferred into the core. Immediately after this pre-loading phase, the processor initiates the computation of the motion vector coordinates for each image macroblock. During this processing stage, the *sin_enable* signal becomes active whenever the last candidate macroblock of the current search area slice is achieved, reporting that a new row of search area pixels should be loaded in parallel to the processor, to prevent the processor to stall. Whenever the end of a given search area is reached, the *data_ready* signal becomes active, indicating that the coordinates of the current motion vector are available to be read at the *output* port. Despite the fact that this *data_ready* signal is active during only a single clock cycle, this motion vector coordinates will remain available for reading until the *data_ready* signal goes active again, during the processing of the next reference macroblock. Figure 4 illustrates the functional operation of the CWdv01, for an implementation with 4×4 pixels macroblock and a search area range constrained to [-4, 5].

Configuration Parameters

N (n_value): dimension of the reference macroblock.

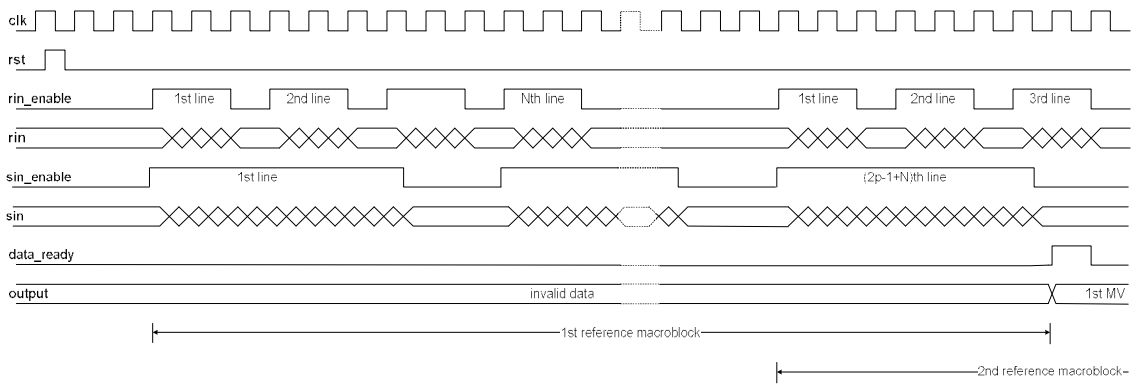

Figure 4. CWdv01 waveforms for an implementation with N=4 and p=5.

P (p_value): maximum allowed displacement in each direction.

Architecture type (SPEED): selection of the architecture that will be used in the description of the processor circuits. Four possible values that can be used for this parameter: 0, 1, 2 and 3. A FPGA oriented architecture can be obtained by setting the SPEED parameter to 0. Setting the SPEED parameter to any of the remaining values generates ASIC oriented descriptions of the processor circuits. Higher values of this configuration parameter generate faster circuit descriptions for all the arithmetic circuits of the processor.

Image height (Nh): horizontal dimension of the input image.

Image width (Nv): vertical dimension of the input image.

Interface Signals

clk (input signal): rising edge clock signal whose frequency is set according to the specified configuration parameters of the core. As an example, for a macroblock width of 8 pixels and a search area range of [-7, +8] pixels, clock frequencies up to 52MHz have been successfully tested.

rst (input signal): asynchronous active high reset signal, used to start the processing.

rin (input signal): reference area pixels input port. Pixels are 8-bit wide.

sin (input signal): search area pixels input port. Pixels are 8-bit wide.

data_ready (output signal): this signal is asserted high ('1') during one clock cycle, when the coordinates of a new valid motion vector are available for reading at the *output* port, and is deactivated ('0') until the next motion vector is available.

data_out (output signal): outputs, in parallel, the 2ω-bit coordinates of the estimated motion vector for each processed macroblock of the reference frame. Note that ω depends on the search range and is given by $\omega=\log_2(p+1)+1$. As soon as *data_ready* rises from '0' to '1', the

coordinates of the motion vector can be read during the subsequent clock cycles, until *data_ready* is activated again for the next macroblock.

rin_enable (output signal): requests a new pixel value from the reference image memory bank. The pixel value **must** be available at the *rin* input in the following clock cycle.

sin_enable (output signal): requests a new pixel value from the search image memory bank. The pixel value **must** be available at the *sin* input in the following clock cycle.