Transient Analysis Modeling of Modular Marx Multilevel Converters

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***Abstract*—This paper presents equivalent models of Modular Marx Multilevel Converter Diode (M^{3}CD) plus load, for bipolar or unipolar operation. With these models, it's possible to analyze and understand the dynamic behavior of the pulse output voltage and current at the load. Simulation and experimental results, for different voltage levels, and various types of load are presented.**

Keywords-Modeling , Multilevel Converter, Pulsed Power.

I. Introduction

The modeling of a Modular Marx Multilevel Converter Diode (M^{3}CD) together with its load is presented in this work. The M^{3}CD can be used as generator of high-voltage positive and/or negative pulses with multi-level voltages lower than the input power supply voltage, as described in [1].

This study can be applied to other multi-level converters based on a half-bridge topology. The half-bridge concept uses two stacks of switching modular cells, one stack in the upper arm and the other in the lower arm. Each modular M^{3}CD cell is derived from the semiconductor based Marx generator [2] and contains two ON/OFF power semiconductors with anti-parallel diodes (or two bidirectional switches), a diode and a capacitor.

The modular M^{3}CD converters may be used in the area of electric power systems (in High Voltage DC transmission, HVDC, for example) or in the area of pulsed power, in applications such as generators of high voltage or as a solution to compensate the generated pulse voltage droop, which could be higher than 10%.

The use of multiple levels for voltage generation is advantageous because it allows the use of kV rated semiconductors to generate tens of kV. The rate of change of the pulse voltage is also reduced enabling the increase of the pulse voltage, without significantly increasing the electromagnetic interference.

The operation principle of M^{3}CD converter contains mainly two steps [3]. The first charges all the capacitors in series (with a fraction of the voltage dc power supply, U_{dc}). The M^{3}CD states are chosen so that in the second step applies the needed voltage level to the load, and the diode interconnecting the modular cells is forward biased placing the capacitors in parallel to balance their voltages [3].

As the M^{3}CD converter uses modular cells it is possible to obtain many voltage levels at the output. The herein presented analysis can be extended to a high number of levels and can be generalized for any converter based on a half-bridge topology.

A multilevel topology M^{3}CD with n levels requires 2(n-1) modular cells [1] to bipolar or unipolar voltages (Fig. 1).

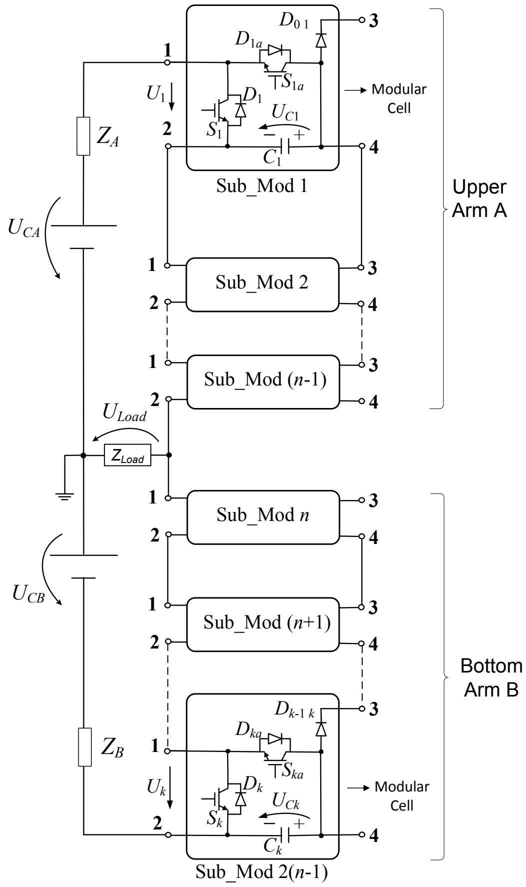


Figure 1. Modulator with n levels using 2(n-1) basic cells.

II. MODELING OF M³CD WITH LOAD FOR BIPOLAR VOLTAGE

The equivalent model of a modulator based on half-bridge topology (Fig. 1) with generic load Z_{Load} for bipolar voltage is shown in Fig. 2, where it is considered the power sources (U_{CA} and U_{CB}), the total impedance of the upper arm A (Z_A), the total impedance of the lower arm B (Z_B) and the load impedance (Z_{Load}).

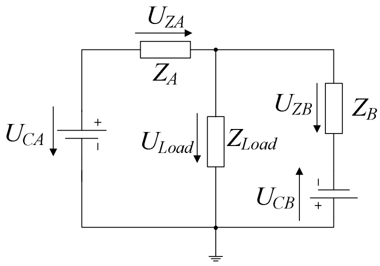


Figure 2. Equivalent model topology half-bridge for bipolar voltage.

To calculate the impedance of each arm, it is considered the equivalent capacitance of the capacitors, which are connected in series for each level, the parasitic resistances (r_1 or r_2) and parasitic inductance (L_1 or L_2), which represent the impedances of the semiconductor and the connections between modular cells.

The impedance value of the upper arm A (Z_A) is given by equation (1), where C_{eqA} are the equivalent capacitance of the capacitors that are connected in series (in upper arm A), and L_1 and r_1 are the parasitic terms of upper arm A components.

$$Z_A = \frac{1}{C_{eqA} s} + L_1 s + r_1 \tag{1}$$

For the bottom arm the impedance value (Z_B) is given by (2), where L_2 and r_2 represent the parasitic terms of bottom arm B and C_{eqB} are the equivalent capacitance of the capacitors that are connected in series (in upper arm B).

$$Z_B = \frac{1}{C_{eqB} s} + L_2 s + r_2 \tag{2}$$

The transfer function of load impedance (Z_{Load}) is obtained depending on the type of load (resistive, resistive capacitive or $R // C$, inductance L in series with $R // C$), to exemplify it was considered an inductance L in series with $R // C$, the impedance value is,

$$Z_{Load} = \frac{RLC_L s^2 + Ls + R}{RC_L s + 1} \tag{3}$$

The parasitic inductors increase the order of the polynomial of the overall system transfer function, while the intrinsic resistors provide little damping. For this reason the output voltage and current responses in capacitive load (parallel RC) are oscillatory with high overshoot.

The models will change accordingly to the voltage level, this is because at each level the number of connected capacitors varies and therefore the impedance of each arm is changed.

Applying Kirchhoff's laws to the equivalent model of Fig. 2 the relationship (4) is received relating the voltage load (U_{Load}) and the voltages sources U_{CA} and U_{CB}.

$$\begin{aligned} U_{Load} &= \frac{Z_B\ Z_{Load}}{Z_B\ Z_{Load} + Z_A\ Z_B + Z_A\ Z_{Load}} U_{CA} + \\ &+ \frac{Z_A\ Z_{Load}}{Z_B\ Z_{Load} + Z_A\ Z_B + Z_A\ Z_{Load}} (-U_{CB}) \end{aligned} \tag{4}$$

In bipolar topology U_{CA} and U_{CB} voltages are approximately equal, $U_{CA} \approx U_{CB} \approx U_{dc}/2$, yielding equation (5):

$$U_{Load} = \frac{Z_{Load}(Z_B - Z_A)}{Z_B\ Z_{Load} + Z_A\ Z_B + Z_A\ Z_{Load}} \frac{U_{dc}}{2} \tag{5}$$

In order to study this mathematic model (5) it was considered a modulator M³CD with 5-level bipolar ($-U_{dc}/4$; $-U_{dc}/2$; 0; $+U_{dc}/4$; $+U_{dc}/2$) working in the level 3, U_{Load}=0V (Fig. 3), however, this study may be applied in other possible combination (i.e. to another voltage level).

A. M³CD with five- level working in the level 3

At this level, two capacitors in upper arm A are connected in series (C_1 and C_2 of Fig. 3), assuming that the capacitance of all capacitors is C then $C_{eqA}=C/2$, S_3 and S_4 are conducting and therefore C_3 and C_4 do not appear in the Z_A impedance.

In bottom arm B, C_5 and C_6 are connected in series ($C_{eqB}=C/2$), switches S_7 and S_8 are conducting and thus C_7 and C_8 do not appear in the Z_B impedance.

The load impedance (Z_{Load}) it is given by equation (3) and corresponds to an inductance L in series with $R // C$.

Replacing the impedances Z_A (1), Z_B (2) and Z_{Load} (3) in equation (5), the equation (6) is obtained:

$$U_{Load} = \frac{As^5 + Bs^4 + Ds^3 + E\ s^2 + Fs}{Gs^5 + Hs^4 + Is^3 + J\ s^2 + Ks + M} \left(\frac{U_{dc}}{2} \right) \tag{6}$$

Where the numerator polynomial coefficients are given in (7):

$$\begin{aligned} A &= C_{eqA}\ C_{eqB}\ R\ LC_L (L_2 - L_1) \\ B &= C_{eqA}\ C_{eqB} L (L_2 - L_1) + C_{eqA}\ C_{eqB}\ R\ L\ C_L (r_2 - r_1) \\ D &= C_{eqA} C_{eqB} R (L_2 - L_1) + C_{eqA} C_{eqB} L (r_2 - r_1) + RLC_L (C_{eqA} - C_{eqB}) \\ E &= C_{eqA} C_{eqB} R (r_2 - r_1) + L (C_{eqA} - C_{eqB}) \\ F &= R (C_{eqA} - C_{eqB}) \end{aligned} \tag{7}$$

This transfer function has a polynomial of 5th order in the numerator with 18 terms and other polynomial of 5th order in the denominator with 36 terms. Looking at the numerator polynomial coefficients (7), if $r_1 > r_2$ or $L_1 > L_2$ or $C_{eqB} > C_{eqA}$, and using the Hurwitz test, this means the numerator of system has at least one root (a zero) in the right half of the complex plane (non-minimum phase system).

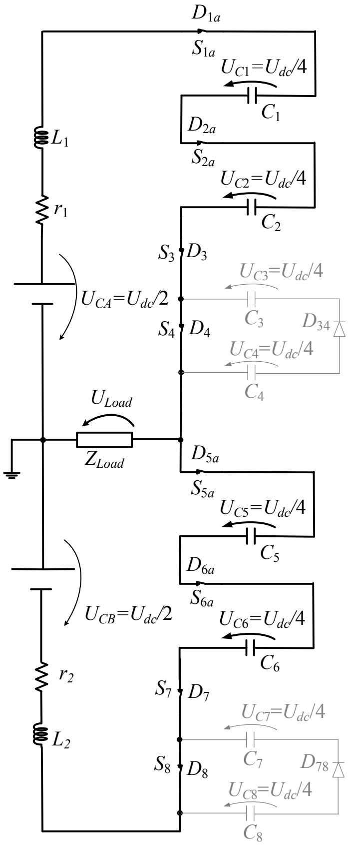


Figure 3. Modulator with five-levels at level 3, U_{Load}=0V.

And the denominator polynomial coefficients are given in (8):

$$
\begin{aligned}
&G = RC_L C_{eqA} C_{eqB} \left(L\,L_1 + L\,L_2 + L_1\,L_2 \right) \\
&H = C_{eqA} C_{eqB} \left(L\,L_1 + L\,L_2 + L_1\,L_2 \right) + \\
&\quad + C_{eqA} C_{eqB} RC_L \left(r_2 L + r_2 L_1 + r_1 L_2 + r_1 L \right) \\
&I = C_{eqA} C_{eqB} \left(R\,L_1 + R\,L_2 + r_1\,L + r_2\,L + r_2\,L_1 + r_1\,L_2 \right) + \\
&\quad + RC_L \left(LC_{eqA} + LC_{eqB} + L_2 C_{eqB} + L_1 C_{eqA} + r_1 r_2 C_{eqA} C_{eqB} \right) \\
&J = RC_{eqA} C_{eqB} \left(r_1 + r_2 \right) + C_{eqA} \left(L + L_1 \right) + C_{eqB} \left(L + L_2 \right) + \\
&\quad + RC_L \left(r_1 C_{eqA} + r_2 C_{eqB} \right) + r_1 r_2 C_{eqA} C_{eqB} \\
&K = r_1 C_{eqA} + r_2 C_{eqB} + R\left(C_{eqA} + C_{eqB} \right) + RC_L \\
&M = 1
\end{aligned}
\tag{8}
$$

It can be seen that the static gain, using the final value theorem, coincides with the expected value for U_{Load} at level 3 is 0V (9). Considering the input value of the system as $U_{dc}/4$ (or $-U_{dc}/4$) the value of the load voltage tends to U_{Load}=0.

$$\lim_{s \to 0} U_{Load}(s) = 0 \tag{9}$$

The load current is obtained as follows:

$$I_{Load}(s) = \frac{U_{Load}(s)}{Z_{Load}(s)} \tag{10}$$

The obtained models for U_{Load} (6) and I_{Load} (10) can be extended to any level number, although it is necessary to adapt the impedances (Z_A and Z_B) which are dependent on the voltage level. The models (6) and (10) may also be adapted for unipolar voltages (U_{CA}=0 for negative pulses or U_{CB}=0 for positive pulses).

III. Simulation and Experimental Results of M^{3}CD with Load for Bipolar Voltage

To validate the study of the dynamic behavior of the mathematical models obtained in section II, simulations and laboratory tests using a M^{3}CD converter with 5 levels (bipolar voltages) were made. To obtain a modulator with five voltage levels (Fig. 3), eight modular cells are needed (four cells for the upper arm and four cells for bottom arm).

In the first set of simulations and laboratory tests the following parameters were used (Table 1):

TABLE I.

U_{DC}=330V (DC SIDE OF THE CONVERTER) STEP VALUE: $U_{DC}/4$=82.5V
$C_{1\text{-}8}$=1μF (CAPACITORS USED IN CELLS)
LOAD WITH INDUCTANCE L=1.25 μH IN SERIES WITH $R//C_L$ WHERE R=20MΩ AND C_L=0.5nF
SIGNAL DESCRIPTION: t_1 =10ms at each intermediate level; width of the minimum and maximum level t_2=t_3=50μs and the interval between pulses t_4 = 500μs.

In Fig. 4 it is observed the bipolar pulse voltage U_{Load} (CH1) with five levels ($+U_{dc}/2$; $+U_{dc}/4$; 0; $-U_{dc}/4$; $-U_{dc}/2$) and the output current I_{Load} (CH2) for an almost complete period.

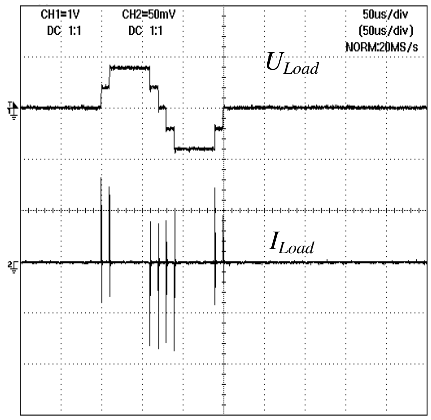


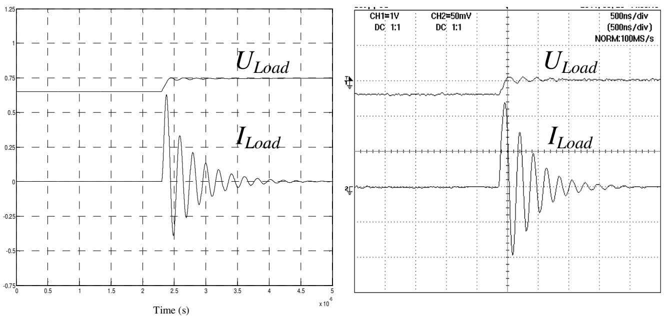
Figure 4. Experimental results of bipolar pulse generator with 5 levels: a) CH1: U_{Load} 200V/div and 50μs/div; CH2: I_{Load} 0.25A/div and 50μs/div.

The simulation goal is to apply the models studied in section II in order to reproduce the dynamic behavior of U_{Load} and I_{Load} when changing the voltage level.

In the first case it was considered the situation of the change of level 2 ($U_{dc} = -U_{dc}/4$) to level 3 (U_{dc} = 0V) (Fig. 4 and Fig. 5). At level 3, two of the four capacitors of upper arm A (associated with the impedance Z_A) are connected in series, in the bottom arm (which are related with impedance Z_B) also two capacitors are connected in series: Equivalent capacitors in upper and bottom arm*:* $C_{eqA}=C/2$= 0.5μF, $C_{eqB}=C/2$= 0.5μF.

The parasitic remaining values L_1, r_1, L_2 and r_2, needed to determine the impedances Z_A and Z_B (measured and estimated values considering 10nH/cm) are: Parasitic inductance of upper arm and bottom arm L_1=1.2μH and L_2=1.2μH; Parasitic resistance of upper arm and bottom arm r_1=50Ω (due to switching semiconductors) and r_2=1.2Ω.

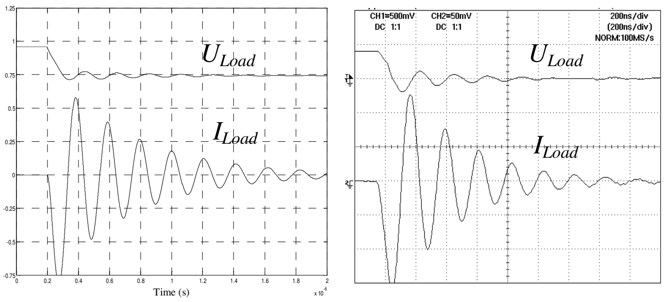
Using the values shown in Table 1 and in the previous text in the models obtained in (6) and (10), the Fig. 5a) illustrates a simulation result of dynamic behavior of U_{Load} and I_{Load} when the pulse voltage level goes from level 2 to level 3. Fig. 5b) shows an experimental result (U_{Load} and I_{Load}) zoom of Fig. 4 of going from level 2 to level 3.



a) b)

Figure 5. Simulation and experimental results of bipolar pulse generator with 5 levels: a) and b) CH1: U_{Load} 200V/div and 500ns/div; CH2: I_{Load} 0,25A/div and 500ns/div.

Fig. 6 shows the simulation and experimental results of switching from level 4 to level 3. A step signal (the set-point) with −82.5V ($-U_{dc}/4$) was applied in this simulation (Fig. 6a). The model used was the same as in Fig. 5 (the initial conditions were not changed). Fig. 6b) shows an experimental result zoom of Fig. 4 switching from level 4 to level 3 for U_{Load} and I_{Load}.

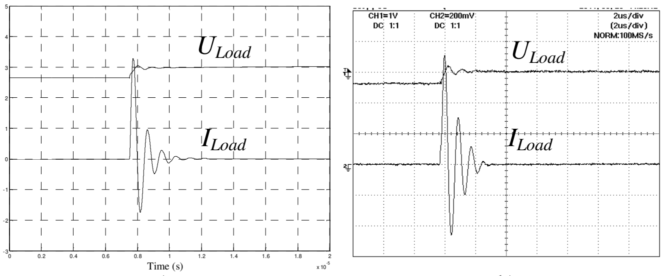


a) b)

Figure 6. Simulation and experimental results of bipolar pulse generator with 5 levels: a) and b) CH1: U_{Load} 100V/div and 200ns/div; CH2: I_{Load} 0,25A/div and 200ns/div.

In a second test, the following parameters were considered: U_{dc}=300V; Load with inductance L=1.1μH in series with $R\,//\,C_L$ where R=40MΩ and C_L=10nF; Capacitors with 1μF and charged with $U_{Ck}=U_{dc}/4$=75V; Signal description: t =10μs at each intermediate level and the interval between pulses t_L = 500μs. The switching from level 2 ($U_{dc} = -U_{dc}/4$) to level 3 (U_{dc} = 0V) was considered (Fig. 7). As mentioned in previous case, to obtain the impedance Z_A, in the level 3, two of the four capacitors of upper arm A are connected in series ($C_{eqA}=C/2$=0.5μF), the same is true for the arm B ($C_{eqB}=C/2$= 0.5μF).

The other values of Z_A and Z_B correspond to parasitic terms, and the values considered (and estimated) were parasitic resistance of upper arm and bottom arm r_1=50Ω and r_2=1.2Ω, parasitic inductance of upper arm and bottom arm L_1=1.2μH and L_2=1.2μH. Using these values Fig. 7a) from simulation closely matches Fig. 7b) from experimental results.



a) b)

Figure 7. Simulation and experimental results of bipolar pulse generator with 5 levels: a) and b) CH1: U_{Load} 200V/div and 2μs/div; CH2: I_{Load} 1A/div and 2μs /div.

IV. Conclusions

This work proposed a new dynamic model for the half bridge based modular Marx multilevel converters. The main objective was the study of the dynamic behavior and the switching times of the output voltage and current. Results obtained in simulation, using the derived mathematical models, and in the laboratory showed reasonable agreement in the transient response of the voltage and current waveforms namely in overshoot and damping values. Therefore, the usefulness of the theoretical analysis is practically verified. The subtle differences may be due to the difficulty in estimating some of the parameters in the real circuit, namely the values of parasitic inductances and semiconductors equivalent resistances.

V. Acknowledgements

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VI. References

[1] L. Lamy Rocha, J. F. Silva, and L. M. Redondo, "Multilevel high voltage pulse generation based on a new modular solid-state switch," IEEE Trans. Plasma Sci., vol. 42, no. 10, pp. 2956–2961, Oct. 2014.

[2] LM Redondo, E Margato, J Fernando Silva, A new method to build a high-voltage pulse supply using only semiconductor switches for plasma-immersion ion implantation, Surface and Coatings Technology 136 (1), pp 51-54.

[3] Rocha, L.; Silva, J. Fernando; Redondo, L.; "Seven Levels Unipolar/Bipolar Pulsed Power Generator", Plasma Science, IEEE Transactions on, (published to IEEE Xplorer in February 2016), doi: 10.1109/TPS.2016.2519269.